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DOCUMENT-IDENTIFIER: US 5579458 A
TITLE: Display control system for a scan type display apparatus

Brief Summary Text (4):
In the ordinary display system which scans a plurality of split display regions in parallel, a random access memory is used as a memory for storing bit map display data to be displayed; and, drawing access for storing display data into the display memory and display access for reading out the stored display data are alternately carried out on a time-sharing basis.

Brief Summary Text (5):
This time sharing display system is able to designate addresses at random during the display access operation and, therefore, to alternately read out the display data from two or more memory regions disposed separately from each other and to supply the plurality of display data to the display device.

Brief Summary Text (8):
The above problem is solved by using a dual port display memory (hereinafter referred to as DPRAM) which is able to execute these two accesses simultaneously. In accordance with this technique, since the reading of data for display from the serial port of the DPRAM is executed by continuous addresses, the display addresses are required to be arranged so as to alternately read the data of plural display regions, for example, an upper display region and a lower display region, from the display memory using a time-sharing system. This means that the display addresses of the plurality of display regions have to be aligned alternately on the basis of the order of the continuous read addresses for the display memory and each data item of the respective display regions should be stored alternately in the display memory during the drawing process.

Detailed Description Text (4):
FIG. 2 shows in detail the architecture of the display control apparatus 304 of FIG. 1. In the embodiment, the display region or display screen 305 (FIG. 1) is divided into two or more split display regions or display screens, for example, upper and lower display regions of the LCD, with the screen size of 32 dots in the horizontal direction and 8 lines in the vertical direction. These two display regions are scanned simultaneously. The display control apparatus 304 (FIG. 1) includes a display memory 102 composed of a dual port random access memory, as shown in FIG. 2. A video random access memory control circuit 101 performs a refreshing of the dual port RAM 102, access control of the serial port and drawing access control via the random access port of the display memory 102 in response to the CPU. A buffer memory control circuit 103 performs address generation control and access control of the buffer memories 104 and 105 for the upper and lower display screen in response to control signals from the display control circuit 101.

Detailed Description Text (6):
As shown in FIGS. 4a, 4b, and 4c, a serial port of the dual port display RAM starts operation in response to a top address being serially accessed and a data transfer cycle control signal (hereinafter referred as a DT cycle) and reads out sequentially the data in response to the serial port reading clock. The display memory control circuit 101 controls these DT cycles, as shown in FIG. 2. The display memory control circuit 101 carries out the drawing processing to the display memory 102 on the basis of an instruction from the CPU 301. First of all, the display data of the first line of the upper display is read out from the display memory 102. That is, the addresses are read out from OH to FH sequentially, as shown in FIG. 3, and are

sequentially stored in the buffer memory 104 for the upper display screen according to the buffer memory addresses and buffer memory writing signals for the upper screen generated by the buffer memory circuit 103.

Detailed Description Text (7):
When one line of data of the upper display region is completely stored in the buffer memory 104, the display memory control circuit 101 starts a DT cycle of the lower display screen and reads sequentially the display addresses from addresses 10H to 1FH and stores them one after another in the buffer memory 105 of the lower display screen.

Detailed Description Text (8):
When the writing process of the buffer memory 105 for the lower display screen is started, buffer memory reading signals of the upper and lower display screens generated by the buffer memory control circuit 103 start the reading process simultaneously from both of the buffer memories 104 and 105 of the upper and lower display screens. Although at this stage, both the reading and writing processes of the display data are executed in parallel for the buffer memory 105 of the lower display screen with time sharing as shown in FIG. 4d to 4g, it is possible to read out the data after completion of writing of the data because the writing is 2 times faster than the reading in processing speed.

Detailed Description Text (9):
When the writing process for the lower display screen is completed, the writing process of the second line for the upper display screen to the buffer memory 104 is started. At this time, the reading process of the display data of the first line for the upper display from the upper display buffer memory 104 continues to be carried out at the same time. More than half of the display data of the first line has been read out at that time point, so the writing of the second line data never goes ahead of the reading of the first line.

Detailed Description Text (12):
In FIG. 5, a determining means 809 compares the value of the vertical display counter 804 with the output value of register 805 and determines whether the set value of the register 805 belongs to the upper display region or the lower display region. Then, it supplies a signal indicating that the vertical split position has been reached on the basis of the result of the determination to the adder subtracter 811 for the upper display addresses or the adder subtracter 812 for the lower display addresses.

Detailed Description Text (13):
A display address generator for the upper display region 806 generates a reading address for the upper display region and a display address generator 807 for the lower display region generates a display address for the lower display region. Register 810 stores an off-set value of the display memory address corresponding to a scroll value when the split display region is scrolled in the vertical direction and the content thereof is supplied to the adder subtracters 811 and 812. The adder subtracters 811 and 812 add or subtract the off-set value of register 810 to or from the memory address of the upper or the lower display region.

Detailed Description Text (15):
A selector 813 controls timing and changes over the outputs of adder subtracters 811 and 812 so as to supply a display reading address for the upper display region and a display address for the lower display region to the display memory 102 alternately.

Detailed Description Text (20):
The vertical display counter 804 renews its count value in proportion to the movement of the display lines from top to bottom. The determining means 809 determines whether the display split position is present in the upper display region or the lower display region. For example, since the display split position of the embodiment is the 6th line in the lower display region, a display split signal to the adder subtracter 811 of the display memory address for the upper display is not rendered active. A vertical splitting signal is generated and is supplied to the adder-subtracter 812 for the lower display region when the vertical display count value reaches a count equal to the difference between the set value of the register

805 and the upper display line number, that is, when the following formula is satisfied.

Detailed Description Text (22):
4: line number of the upper display region

Detailed Description Text (24):
The set value "4" of the register 810 is added to the display memory address of the lower display region by the adder subtracter 812. As a result, the display memory address is varied from 14H to 18H. Hereinafter, the display memory address is increased by "4" as shown in FIG. 6. All lines after the 6th are shifted or scrolled by one line, but the lines of the upper display region are not shifted or scrolled.

Detailed Description Text (26):
As described with reference to the embodiment the present invention, the address map set by the CPU is the same as that of the time sharing system using the ordinary random access memory, and therefore, the same drawing processing software is applicable to the present invention without change of the drawing method.

Detailed Description Text (27):
Furthermore, the ordinary time sharing system executes the drawing access and display access operations to the display memory through only one port. On the other hand, the present invention carries out the drawing access and display access operations through separate ports of the dual port display memory. As a result, the speed of the drawing process becomes fast because the competition between the drawing access and display access is avoided. Despite using the dual port memory as the display memory, high speed partial scrolling of the display screen is ensured.